

Pull-up circuit

This invention relates to a pull-up circuit, and in particular to a pull-up circuit which is suitable for use in a USB device.

Electronic devices can be interconnected by means of a Universal Serial Bus (USB), and the USB specifications specify various required features of USB-compatible
5 devices.

The USB specifications specify two possible operating speeds for USB Devices, defined as full speed and low speed. The USB specifications then further specify two pins which are provided on USB Devices, for connection to respective bus lines, and require that a USB Device should pull one of the bus lines to a particular voltage when the
10 bus line is in an idle state. If the D+ pin is pulled up to the required voltage, this indicates that the Device can operate at full speed, whereas, if the D- pin is pulled up to the required voltage, this indicates that the Device can only operate at low speed.

It is desirable to make battery powered portable devices USB-compatible, but such devices typically have low voltage power supplies, which makes it difficult for such
15 devices to pull the required bus lines to the specified voltage.

In some cases, the required voltage can be provided from the bus voltage. However, the USB specifications also define on-the-go (OTG) devices, which can act either as a USB host or as a peripheral. Such devices cannot be powered exclusively by the bus voltage because, when they are acting as hosts, they must supply the bus voltage. In the case
20 of USB OTG devices, therefore, there are specific factors which must be taken into consideration.

Moreover, integrating the pull-up circuit into the USB Device means that resistors can only be implemented with wide tolerances. This places further constraints on the form of the pull-up circuit.

25 According to the present invention, there is provided a pull-up circuit, comprising an operational amplifier which forms part of a feedback circuit, acting to bring a pull-up circuit output equal to a reference voltage input.

According to another aspect of the present invention, the pull-up circuit forms part of a USB transceiver for incorporation in a USB Device. When the supply voltage of the

USB Device is sufficiently high, it is used to provide the required pull-up voltage, with the feedback circuit including the operational amplifier being enabled only when the supply voltage of the USB Device is not high enough to provide the required pull-up voltage. In that case, the USB bus voltage is used to generate the reference voltage which is used as an input
5 to the feedback circuit.

Fig. 1 is a schematic diagram of a USB OTG device in accordance with an aspect of the present invention.

10 Fig. 2 is a circuit diagram of a pull-up circuit, in accordance with another aspect of the present invention, in the USB device of Fig. 1.

Fig. 1 shows a USB Device in accordance with a first aspect of the present
15 invention.

In this preferred embodiment of the present invention, the USB Device is a dual-role on-the-go (OTG) Device, as defined in the USB specifications, meaning that it can act as a USB Host or as a USB Peripheral, depending on the circumstances of its use. However, the invention is equally applicable to other USB Devices.

20 Thus, Fig. 1 shows a USB OTG Device 10, having a functional block 12, which performs many of the desired operational functions of the USB Device. For example, the USB Device 10 may be a microprocessor or a digital signal processor, in which cases the functional block 12 performs the functions of the microprocessor or digital signal processor.

The USB Device 10 also includes a USB transceiver 14, which has a role in
25 configuring the connection of the USB Device 10 over a USB bus to another such Device. The USB Device 10 also has a USB connection, including a bus pin Vbus, and bus lines D+ and D-. The signals on the D+ bus line 16 and the D- bus line 18 indicate the status of the USB Device 10 to the other USB Device.

More specifically, when the D+ bus line 16 or the D- bus line 18 is pulled up
30 to a specified voltage, in the range from 2.7V – 3.6V, this indicates that the USB Device 10 is acting as a USB Peripheral. When the D+ bus line 16 and the D- bus line 18 are pulled down, by closing the switches 20, 22, and connecting the bus lines to ground through the respective resistors 24, 26, this indicates that the USB Device 10 is acting as a USB Host. When it is the D+ bus line 16 which is pulled up or down in this way, this indicates that the USB Device 10

can operate at full speed, as defined in the USB specifications. When it is the D- bus line 18 which is pulled up or down in this way, this indicates that the USB Device 10 can operate at low speed, as defined in the USB specifications.

As described so far, the USB Device 10 is generally conventional, and so the other functions and features of the device will not be described in further detail.

Fig. 2 shows in more detail the form of a pull-up circuit in the USB transceiver 14. In preferred embodiments of the invention, the USB transceiver can be provided as an integrated circuit, which includes two such pull-up circuits, and also includes the pull down resistors 24, 26 and their associated switches 20, 22, plus a DC-DC regulator for forming a regulated voltage Vreg (for example at 3.3V) from the supply voltage Vbat of the USB Device 10. The USB transceiver 14 preferably also includes other circuitry, which can be of a type which is generally known, for performing other required features. For example, the USB transceiver 14 preferably also includes circuitry for forming an identification signal, and circuitry for monitoring and pulsing the bus line.

As also shown in Fig. 1, the USB transceiver receives as inputs the bus voltage Vbus, a bias current I_{bias} from the functional block 10, plus logic signal inputs PU_EN* and IDLE, also from the functional block 10. Fig. 2 shows the form of the pull-up circuit connected to the D+ line 16. Thus, in the USB transceiver 14 there is another such pull-up circuit, connected to the D- line 18.

The logic signal input IDLE is high when the USB Device 10 is in the idle mode. In this situation, it is required that the USB Device should indicate whether it can act as a USB Host or a USB peripheral, and whether it can operate at full speed or only at low speed. The logic signal input PU_EN* is low when this pull-up circuit is required to operate. Thus, in the case of this pull-up circuit connected to the D+ line 16, this logic input is low when the USB Device can act as a USB Peripheral at full speed.

Thus, when the USB Device 10 is acting as a USB Host, the pull-down resistors 24, 26 are both activated, by closing the switches 20, 22. The USB Device can then detect whether another connected USB Device is operating at full speed or at low speed, by sensing which of its pull-up resistors is activated. When the USB Device 10 is acting as a USB Peripheral, one of the two pull-up circuits is activated. The pull-up circuit connected to the D+ line 16 is activated when the USB Device is operating at full speed, and the pull-up circuit connected to the D- line 18 is activated when the USB Device is operating at low speed.

The pull-up circuit shown in Fig. 2 is connected to the D+ line 16, and will be described further on that basis, but the pull-up circuit connected to the D- line 18 is essentially identical, although the logic signals operate to ensure that the appropriate one of the circuits is activated as required.

5 The supply voltage Vbat of the USB Device 10 is applied to a comparator block 32, which determines whether the supply voltage Vbat exceeds 3V. The output of the comparator block 32, and the logic signal inputs PU_EN* and IDLE are applied to logic circuitry 34. When the supply voltage Vbat is lower than 3V, the logic circuitry 34 acts such that the output voltage, on the D+ bus line 16, is generated by active pull-up circuitry 36 from the bus voltage Vbus. However, when the supply voltage Vbat exceeds 3V, the active pull-up circuitry 36 is not required, and the output voltage, on the D+ bus line 16, is generated from the supply voltage Vbat by alternative pull-up circuitry 37.

 The active pull-up circuitry 36 includes an operational transconductance (OTA) amplifier 38, which receives a reference voltage Vref on its non-inverting input terminal. The reference voltage Vref is generated from a string of five diodes 40, 42, 44, 46, 15 48, connected in series between the bus voltage Vbus and ground. As is known, the resistances of the diodes 40, 42, 44, 46, 48 depend on their respective width/length (W/L) ratios, and these can be adjusted such that the reference voltage Vref takes a desired value. For example, for a nominal bus voltage of 5V, a value of the reference voltage Vref in the region of 3.1V - 3.2V will usually be sufficient, as, with a +/- 10% variation on the bus 20 voltage, this will ensure that the reference voltage Vref still falls within the range of 2.7V - 3.6V specified for the pull-up voltage on the D+ bus line 16. Typically, the resistance of the diodes 40, 42, 44, 46, 48 will be high enough that there will be minimal current leakage (for example, a maximum of 2μA) through the diodes.

25 The output terminal 50 of the OTA amplifier 38 is connected to the gate of a first NMOS transistor 52. The drain of the first NMOS transistor 52 is connected to the bus voltage Vbus, while the source of the first NMOS transistor 52 is connected to the D+ bus line 16, which is also connected to the inverting input of the OTA amplifier 38.

 A first PMOS transistor 54 has its drain connected to the bus voltage Vbus, 30 and its source connected to the output terminal 50 of the OTA amplifier 38. The gate of the first PMOS transistor 54 receives a logic signal from the logic circuitry 34, which is also supplied to an enable input of the OTA amplifier 38.

 The alternative pull-up circuitry 37 includes a second PMOS transistor 56, having its drain connected to the regulated voltage Vreg (for example at 3.3V), which is

formed from the supply voltage Vbat of the USB Device 10, and its source connected to the D+ bus line 16 through a first pull-up resistor 58. The gate of the second PMOS transistor 56 receives a second logic signal from the logic circuitry 34.

The alternative pull-up circuitry 37 also includes a third PMOS transistor 60, having its drain connected to the source of the second PMOS transistor 56, and its source connected to the D+ bus line 16 through a second pull-up resistor 62. The gate of the third PMOS transistor 60 receives a third logic signal from the logic circuitry 34.

In the logic circuitry 34, the logic signal input PU_EN* is connected through a first inverter 64 to a first input of a first OR gate 66. The logic signal input IDLE is connected to a second input of the first OR gate 66.

The output of the first OR gate 66 is connected to a first input of a NAND gate 68. The output of the comparator block 32 is connected to a second input of the NAND gate 68.

The output of the comparator block 32 is also connected to a first input of a NOR gate 70. The output of the first OR gate 66 is connected through a second inverter 72 to a second input of the NOR gate 70.

The logic signal input PU_EN* is also connected to a first input of a second OR gate 74. The output of the NOR gate 70 is connected to the second input of the second OR gate 74.

The output of the NOR gate 70 forms the first logic signal input to the active pull-up circuitry 36, specifically to the gate of the first PMOS transistor 54 and the enable signal input of the OTA 38. The output of the second OR gate 74 forms the first logic signal input to the alternative pull-up circuitry 37, specifically to the gate of the second PMOS transistor 56. The output of the NAND gate 68 forms the second logic signal input to the alternative pull-up circuitry 37, specifically to the gate of the third PMOS transistor 60.

The logic circuit therefore operates such that, when the logic signal input PU_EN* is low, and the logic signal input IDLE is high, the pull-up circuit is activated, to place a voltage within the range of 2.7V – 3.6V on the D+ bus line 16, and thereby indicate that the USB Device can act as a USB Peripheral at full speed.

More specifically, in operation of the device, when the logic signal input IDLE is high and the supply voltage Vbat exceeds 3V, it is determined that the supply voltage is sufficient to provide the output voltage on the D+ bus line 16. Thus, when the comparator block 32 determines that the supply voltage Vbat exceeds 3V, the first logic signal input to the active pull-up circuitry 36, specifically to the enable signal input of the OTA 38, is low.

Therefore, the OTA 38 is disabled. At the same time, the first and second logic signal inputs to the alternative pull-up circuitry 37, specifically to the gates of the second and third PMOS transistors 56, 60 respectively, are also low. As a result, the PMOS transistors 56, 60 are turned on, and the voltage on the D+ bus line 16 is brought up towards the level of the regulated voltage Vreg obtained from the supply voltage Vbat, with the resistance values of the resistors 58, 62 being such that the voltage drop across them is sufficiently small that the voltage on the D+ bus line 16 is at least 2.7V for all values of the supply voltage Vbat greater than 3V.

The voltage drop across the resistors 58, 62 depends on the combined resistance of the resistors 58, 62, and on the resistance value of the pull-down resistor 124 in the device which is acting as the USB Host. In accordance with the USB Specification Revision 2.0, USB Engineering Change Note, this pull-down resistor should have a value in the range 14.25kohm – 24.8kohm. This means that the idle voltage is pulled up almost to the regulated voltage Vreg.

When the logic signal input IDLE is low, however, that is, the device is in the active state rather than the idle state, it is not necessary to maintain the idle voltage, but it is disadvantageous for the pull-up resistance to be too low, as this adversely impacts quality of the transmitted signals. In that case, the logic circuitry operates to switch the resistor 62 out of the circuit, so that the value of the pull-up resistance is increased. According to the USB Specification Revision 2.0, USB Engineering Change Note, the value of the pull-up resistance shall be in the range 900ohm – 1575ohm when the device is in the idle state, and in the range 1425ohm – 3090ohm when the connected USB Host Device is in the active state.

When the comparator block 32 determines that the supply voltage Vbat is lower than 3V, the first and second logic signal inputs to the alternative pull-up circuitry 37 are high. As a result, the PMOS transistors 56, 60 are turned off. At the same time, the first logic signal input to the active pull-up circuitry 36, specifically to the enable signal input of the OTA 38, is also high. Therefore, the OTA 38 is enabled. Meanwhile, the gate of the first PMOS transistor 54 is also brought high, so that this transistor is switched off.

The OTA 38 therefore forms the basis for a feedback circuit, which acts to bring the voltage on the D+ bus line 16 to the level of the reference voltage Vref, since, as is usual with operational amplifiers, the non-inverting input and the inverting input of the OTA must have the same voltage level. More specifically, the first NMOS transistor 52 acts as a current source, which is controlled by the OTA 38, and therefore maintains the voltage on the D+ bus line 16 at the level of the reference voltage Vref.

Since the active pull-up circuitry 36 includes a feedback loop, it is necessary to consider its stability. Fig. 2 shows the capacitance on the D+ bus line 16 as a capacitor 76, having a capacitance value C1. In practice, the capacitance value C1 can lie anywhere in the range from 0pF – 1000pF, and so it is necessary that the feedback loop should include an
5 internal dominant pole, so that the stability of the feedback loop does not depend on the capacitance value C1. In this preferred embodiment of the invention, this is achieved by including a Miller capacitor having a value of 4.5pF in the OTA.

In this preferred embodiment of the invention, the pull-down resistors 24, 26 shown in Fig. 1, are also integrated into the USB transceiver 14. If the USB Device 10 is
10 acting as a USB Host, the switches 20, 22 are closed, in order to activate the resistors 24, 26.

There is therefore provided a pull-up circuit, and an associated USB transceiver circuit, which ensure that the voltage on the D+ line (or D- line, as required) of a USB Device is maintained at the required level, even for low voltage devices, despite possible variations in the available bus voltage.

15 The pull-up circuit according to the preferred embodiment of the invention determines whether the available battery voltage is sufficient to provide the required voltage on the D+ or D- line, and activates active pull-up circuitry only in the event that the available battery voltage is insufficient. However, the active pull-up circuitry based around the OTA 38 can also be used in USB Devices without having available the option of using the battery
20 voltage to provide the required voltage on the D+ or D- line.

It will also be apparent to the person skilled in the art that other changes may be made to the circuit, without altering fundamentally the operation thereof. For example, some or all of the PMOS and NMOS transistors in the active pull-up circuitry can be replaced by NMOS or PMOS transistors, as the case may be, with appropriate changes to the applied
25 logic signals.